# Low Power Nine-bit Sigma-Delta ADC Design Using TSMC 0.18micron Technology

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***Abstract*—In Sigma-Delta analog to digital conversion method, the input signal is represented by a sinusoidal signal of magnitude 1V at a signal band of 1MHz.The modulator is operated with ±1.8V supply voltage and a fixed oversampling ratio of 128. The CIC filter designed includes integrator, differentiator blocks and a dedicated clock divider circuit, which divides the input clock by 32. It achieves a resolution of 9-bits by occupying silicon chip area of 8043µm$^2$ and by consuming a total power of 540.48nW. A first order sigma-delta modulator, which is implemented using TSMC 180nm technology using Mentor Graphics Pyxis tool and the second order CIC decimation filter is implemented in Verilog HDL.**

***Keywords—OSR; Op-amp; First order modulator; CIC Decimation filter; Xilinx.***

## I. INTRODUCTION

Sigma-Delta ADC is a mixed signal circuit block, which is suitable for on chip VLSI implementation. Applicationof mixed signal systems are continuously increasing in an effort to bring the whole system in a chip. The recent technological advances now make the sigma-delta converters practical and their use is becoming widespread and is more advantageous for mixed-signal system realizations. Sigma-delta ADC is a low-cost, low power, high-resolution ADC and has various applications in signal processing, communications systems, consumer and professional audio, industrial weight scales.

A sigma-delta ADC comprise of an analog block of first order modulator and digital block of second order decimator. Sigma-delta modulation is widely used in the field of analog to digital conversion [1], [2], [6]. The basic technique used by the sigma delta modulator are (1) oversampling [1], [2]. It is the technique in which it samples the signal at a rate higher than nyquist rate. Normally this is used to eliminate the requirement of anti-aliasing filter. (2) Noise shaping [4], which shapes the quantization noise by pushing it towards high frequency band and can be filtered out by using digital decimation filter. Decimation process is used to extracts the information from the data stream and eliminate the redundant data at the output. The bit stream is digitally filtered and down sampled by a factor of M i.e., it selects one sample out of M samples from the signal. In this paper down sampling and low pass filtering is successfully done by using CIC (cascade integrated comb) filter, which was proposed by Eugene Hogenauer in 1981 [5].

The number of individual CIC filters useddetermines the order of the CIC filter. For a sigma-delta modulator of order L, a cascade of k= L+1 comb filters is needed to adequately attenuate the quantization noise that would alias into the desired band [12]. This filter is area and power efficient for hardware implementation. The CIC filter does not require any multiplier because the filter coefficients are all unity. So, there is no storage space is required for filter coefficient. It avoids the data loss due to register overflow.

The paper describes the basic principles and architecture of complete SD ADC in Section II. In section III, the detailed design of Sigma-delta modulator is described, providing transistor level design and circuit simulations of the op-amp and comparator. The basics of cascaded Integrator combdecimation filter and its floor plan are presented in section IV. The output results of the SD ADC and its response are also discussed in this section. The section V represents synthesis results of total ADC. The conclusion and future work is discussed in section VI.

## II. ARCHITECTURE OF SIGMA-DELTA ADC

Now a days therecent technological advancement in sigma delta conversion technique makes the devices more practical and widespread.

The Σ-Δ ADC architecture had its origins in the early development phases of pulse code modulation (PCM) systems those related to transmission techniques called delta modulation and differential PCM. Delta modulation was first invented at the ITT Laboratories in France by E. M. Deloraine, S. Van Mierlo, and B. Derjavitch in 1946 [12].

The design of sigma-delta ADC includes first order oversampled sigma-delta modulator and digital decimation filter.The sigma-delta ADC architecture is shown in Figure 1 where analog front-end is oversampled noise shaping modulator, which is used to digitize the analog input signal with a very low resolution (i.e., 1 bit) at a very high sampling rate. The output of modulator not only contains the signal but also the high frequency quantization noise. Digital back-end is decimation filter, which removes these high frequency quantization noise.

The Σ-Δ ADC can also be viewed as a synchronous voltage-to-frequency converter followed by a counter.

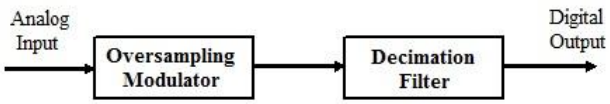


Figure 1. Block diagram of sigma-delta ADC

If the number of "1"s in the output data stream is counted over a sufficient number of samples, the counter output will represent the digital value of the input. Obviously, this method of averaging will only work for dc or very slowly changing input signals. In addition, $2^N$ clock cycles must be counted in order to achieve N-bit effective resolution, thereby severely limiting the effective sampling rate.

It should be noted that there is a built-in "pipeline" delay (often called "latency") that is determined by the number of taps in the digital filter because the digital filter is an integral part of the Σ-Δ ADC. Digital filters in Σ-Δ ADCs can be quite large (several hundred taps), so the latency may become an issue in multiplexed applications where the appropriate amount of settling time must be allowed after switching channels.

## III. SIGMA-DELTA MODULATOR

The sigma-delta modulation was developed basing upon the well-established delta modulation [7]. Δ-modulation shapes both noise and signal equally and quantizing the change in the signal from sample to sample rather than the absolute value of the signal at each sample [8]. Due to this disadvantages sigma-delta modulation is preferred.

The name Sigma-Delta modulator comes from putting the integrator (sigma) in front of the delta modulator. Sometimes, it is referred to as an interpolative coder [9]. The arrangement shown in Figure 2 is called a Sigma-Delta Modulator. It consists of an integrator and a 1-bit ADC in the forward path and a 1-bit DAC is in the feedback path. In the sigma-delta modulator, the difference between analog input signal and the output of 1bit DAC is given to the input of integrator The integrator is typically a switched capacitor integrator and the 1-bit ADC is a normal comparator which converters an analog signal to either 'high' or 'low'. The number of integrators in the forward path determines the order of the modulator. 1-bit DAC is a simple multiplexer circuit controlled by the output of the comparator.

When the integrator output is greater than the reference voltage at the comparator input, the comparator gives an output 'high'. This output high controls the DAC which gives an output of +Vref which is subtracted from the input of the modulator in order to move the integrator output in the negative direction.

Similarly when the integrator output is less than the reference voltage at the comparator input, the feedback path moves the integrator output in the positive direction. The integrator therefore accumulates the difference between the input and quantized output signals and tries to maintain the integrator output around zero. A zero integrator output implies that the difference between the input signal and the quantized output is zero. Thus the average value at the output will be equal to the value at input.

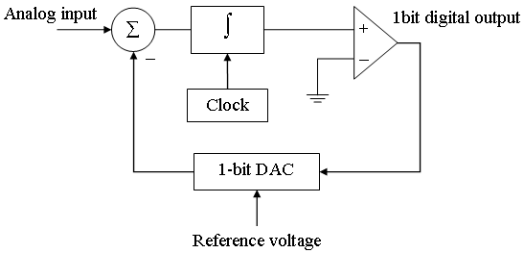


Figure 2. Block diagram of sigma-delta modulator

### A. *Two stage CMOS op-amp*

The two stage circuit is the most popular approach for both bipolar and CMOS op-amps, where a complementary process that has reasonable n-type and p-type devices is available. When properly designed, the two stage op-amp has performance very close to more modern designs.

To achieve better stability, the designed op-amp should have large gain and phase margin. A two-stage CMOS operational amplifier topology is used as shown in the Figure 3, which consists of a differential input stage followed by a second gain stage. An output stage is usually not used but maybe added for driving heavy loads off-chip.

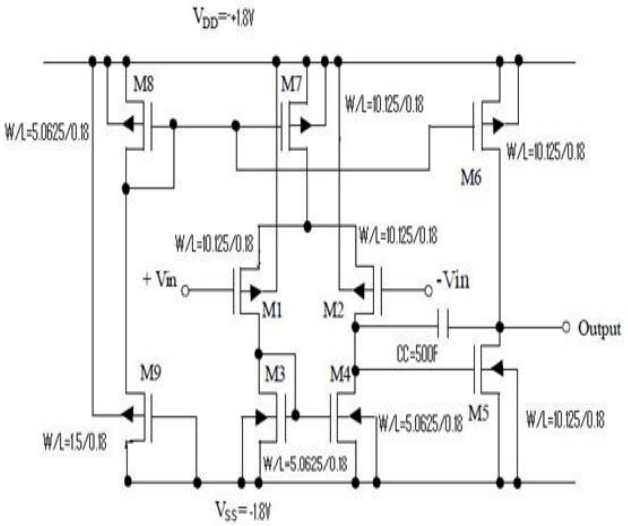


Figure 3. Two stage CMOS op-amp

Figure 4, shows the frequency response characteristics. In this design, the DC gain of the amplifier is found to be 82 dB and phase margin is 78 degree. Fig.5 determines the slew rate of the op-amp. As already said the higher is the slew rate, the better is the response of the op-amp. From the Fig 5 the slew was found to be 1019V/μsec.

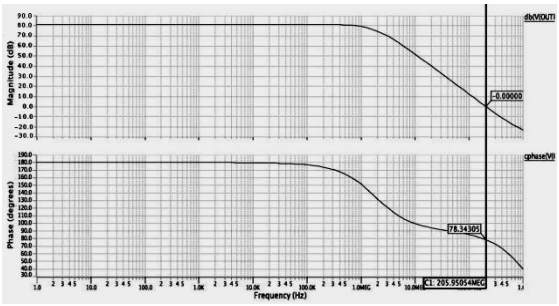


Figure 4. Frequency response of two stage op-amp

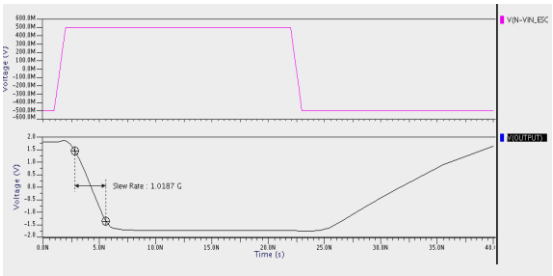


Figure 5. Slew rate of two stage op-amp

*B. Two stage CMOS comparator*

The comparator is mainly used to convert analog signal to digital signals. The sampled signal is applied to comparators to determine the digital equivalent of the analog signal. Comparator can be considered as a 1-bit ADC, which has two levels either a '1' or a '0'. A '1' implies that $V_{DD}$ =+1.8V and a '0' implies that $V_{SS}$ = -1.8V.

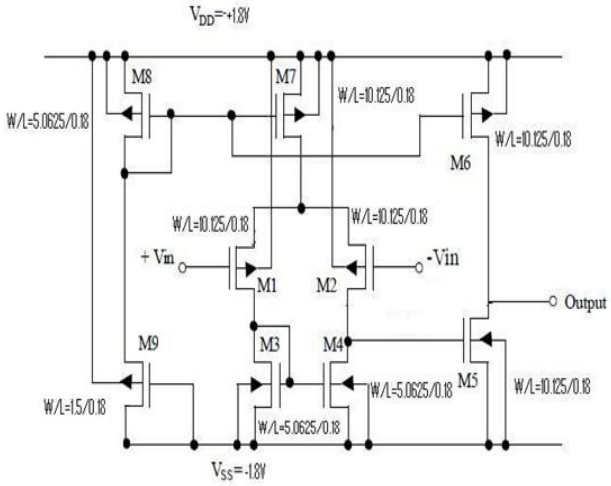


Figure 6. Two stage CMOS comparator

In case of A/D converter, the comparator must slew its output quickly without oscillation once it crosses the input thresholds. The comparator circuit is shown in Fig. 6. Comparators are characterized by their voltage gain, slew rate and an offset voltage for a given over drive.

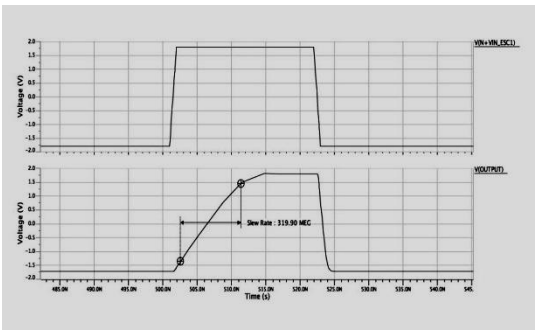

Figure 7. Slew rate of two stage comparator

The clock frequency of the first order modulator depends on the slew rate of the comparator. The slew rate for the comparator is measured by giving a step input signal. Assuming a 3pF load at the output of the comparator the slew rate is around 320 V/**µ**S as shown in Fig 7. The clock frequency should be less than the slew rate of the comparator.The maximum allowed clock frequency for the desired slew rate would be 250MHz in this design. When the clock frequency is more than 250MHz, the comparator output will be distorted.

In sigma-delta modulator, the analog input is a sine wave and the output is 1-bit digital data. In each clock cycle, the value of output of modulator is either plus or minus full scale, according to the results of the 1-bit A/D conversion. When the sinusoidal input to the modulator is at the peak of positive full scale, the positive pulse width of the output is high. When the input is close to the minus full scale, the negative pulse width of the output is high. When the input reaches zero the positive pulse width becomes equal to the negative pulse width and varies rapidly between a plus and minus full scale shows in Fig. 8.

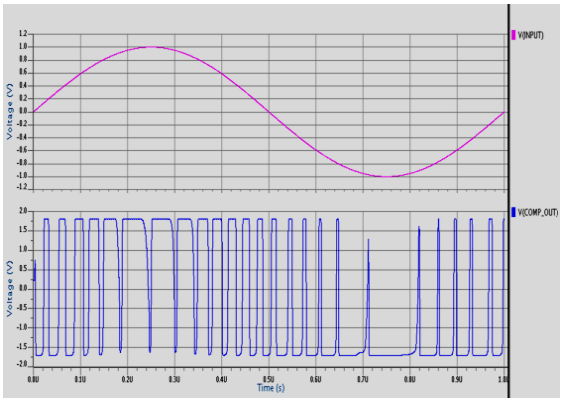


Figure 8. Input and output of first order sigma-delta modulator

## IV. DECIMATION FILTER

The decimation process can be used to provide increased resolution. This filter is the combination of low pass filter and down sampler. Its main function is to extract the information from the data stream and remove the high frequency quantization noise.

One of the successful way of implementing the decimation filter is by using Cascaded Integrator Comb (CIC) filter. The CIC filter consist cascade of integrators and comb filters by connecting down sampler of K stage as shown in Fig. 9. The stage of integrator and comb section is used to determine the order of CIC filter.

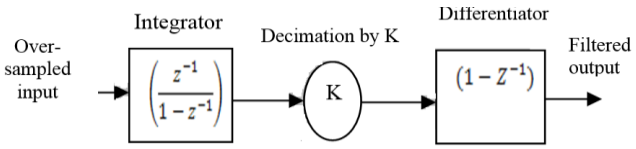


Figure 9. Block diagram of CIC as decimation filter

This filter consists of two digital integrators followed by two comb filters. The proposed architectural view of CIC filter is shown in fig.10.

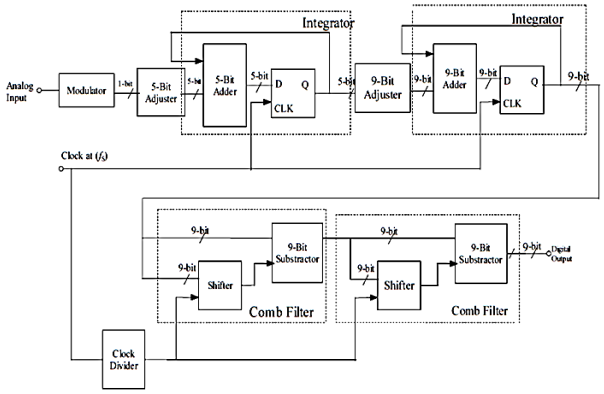


Figure 10. Architecture of proposed two stage CIC filter.

The 5-bit adjuster and the 9-bit adjuster are simple multiplexer circuits, which performs the bit adjustment as required. This 5-bit adjuster converts the 1-bit modulator

output to 5-bits. It is a 2-to-1 multiplexer by appending either 0's or 1's to the modulator output. Similarly, the 9-bit adjuster converts the output of the first integrator stage to 9-bits.An integrator stage is obtained by using a delay element and an adder. Here the delay elements are designed using a D flip-flop. Integrator is also known as an accumulator which is used to store the sum of the input data. The comb filter is called as differentiator, which is also a finite impulse response digital filter (FIR). This stage is obtained by using a shifter and a subtractor. The shifter is a simple cascade of four 9-bit registers, which is implemented using D flip-flops. The clock divider decreases the clock frequency by OSR/4 times and is then applied to the differentiator circuit of the CIC filter [10].In this case, the clock frequency is decreased by 32 times to 8MHz where the input at $n^{th}$ instant is subtracted from the output of the shifter which will be the $(n-128)^{th}$ instant.

Sigma-delta ADC is operated is at 1 MHz, the output occurs at 8 MHz, so input signal has a time period of 1µs, and the output takes 0.125µs to complete one cycle. For sigma-delta ADC 1 LSB is defined as [11].

$$1\ \text{LSB}=\frac{V_{FSR}}{2^N}$$

Where $V_{FSR}$ is the full scale voltage range of the input signal and N is the number of output bits. The LSB value is generally used for finding the analog equivalent value of the digital output. The decimal equivalent is obtained by multiplying the bit coefficient with the respective powers of 2.The analog equivalent can be calculated by multiplying the decimal equivalent value with the value of 1 LSB.

The analog equivalents are in the voltage range from (0 to 2)V, but to represent the actual input voltage which ranges from -1 V to + 1 V, there is a drop of 1 V is required in the analog equivalent value, which is shown in the Table I. The experimental output results for first order sigma-delta ADC is shown in Fig.10 using the labels OUT (0) through OUT (9) where OUT(9) represents the MSB value and OUT(0)represents the LSB value.

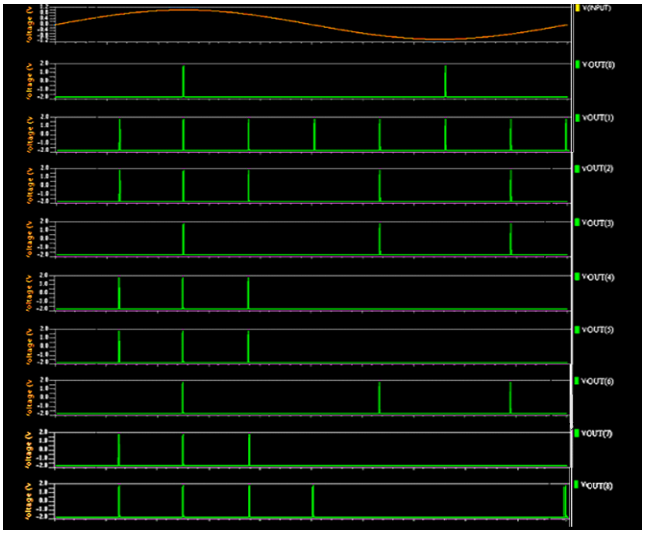

Figure 11. Output waveforms of first order sigma-delta modulator.

The analog equivalent that is calculated from the multi bit digital decimated output is nearly equal to that of input sine wave value of analog signal.

TABLE I. TABULAR DATA REPRESENTATION OF THE 9-BIT DECIMATOR OUTPUT FOR K = 32 CASE

| Analog input voltage (volts) | Output digital code | Decimal equivalent | Analog equivalent (A) | Actual Analog Voltage (A –1V) (volts) |
|---|---|---|---|---|
| 0.7 | 110110110 | 438 | 1.7108 | 0.7108 |
| 1 | 111111111 | 511 | 1.9959 | 0.9959 |
| 0.7 | 110110110 | 438 | 1.7108 | 0.7108 |
| 0 | 100000010 | 258 | 1.0077 | 0.0077 |
| -0.7 | 001001110 | 78 | 0.3046 | -0.6954 |
| -1 | 000000011 | 3 | 0.0117 | -0.9882 |
| -0.7 | 001001110 | 78 | 0.3046 | -0.6954 |

## V. SIMULATION RESULTS

The sigma-delta ADC includes the analog block for modulator part and digital block for demodulator part. Total ADC was implemented using TSMC 180 nm technology. The CIC filter of digital part is used to achieve the resolution of 9-bit by occupying the cell area of 8043µm$^2$and consumes total power of 540.48nw. The floor plan of cascade integrated comb filter is shown in fig.11, which requires the gate count of 150 and provides the delay of 2.67 ns. In analog part the achieved gain and slew rate of op-amp was 82dB and 1019V/µs respectively. The performance is summarized in Table II.

TABLE II. PERFORMANCE SUMMARY OF SIGMA-DELTA ADC

| Performance | Value | Comment |
|---|---|---|
| DC gain | 82dB | of OPAMP |
| Slew rate | 1019V/**µ**S | of OPAMP |
| Phase margin | 78 degree | of OPAMP |
| Input signal frequency | 1MHz | of SD ADC |
| Input supply voltage | 1.8V | of SD ADC |
| Slew rate | 320V/**µ**S | of Comparator |
| Gate count | 150 | of CIC Filter |
| Cell area | 8043**µ**m$^2$ | of CIC Filter |
| Power consumption | 540.484nW | of CIC Filter |
| Delay | 2.67ns | of CIC Filter |
| Technology | TSMC180nm | of SD ADC |

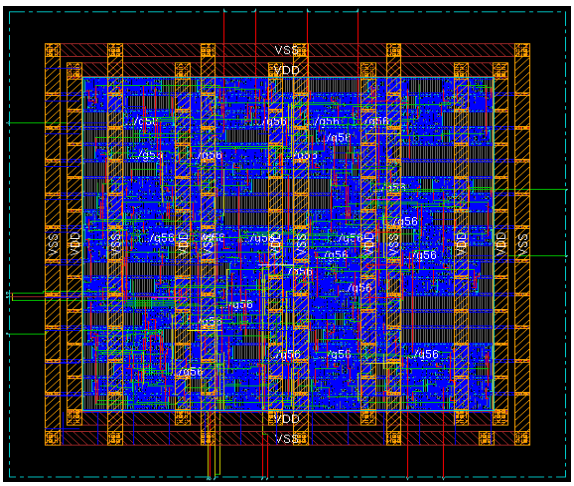

Figure 12. Floor plan of second order CIC filter.

## VI. CONCLUSION

Sigma-delta conversion technology is based on oversampling, noise shaping and decimation filtering, which offers system cost saving because it avoids the requirement of

analog anti-aliasing filter. Since digital filtering follows the A/D conversion, noise (i.e. voltage reference noise, power supply ripple) injected during the conversion process, can be controlled. The complete sigma delta ADC is designed using a first order modulator and a second order CIC Decimation filter with an oversampling ratio of 128. The decimator output is a 9-bit digital output. Using this efficient circuit design the power consumption decreases to a value up to540.48nW. it is based predominantly on digital signal processing, hence the cost of implementation is low and will continue to decrease. Also, due to the digital nature, sigma-delta converters can be integrated onto other digital devices. Attaining a high level of performance at a fraction of cost of hybrid and modular designs is probably the greatest advantage of all.

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